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Integrierte Schaltung

Circuit intégré

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an integrated circuit having a function for enabling a mode of a circuit to be switched over if a predetermined signal is input to a mode switching signal input terminal in condition where predetermined voltage is applied to one or more signal input terminals.

2. Prior art and related reference

In a conventional integrated circuit, a semiconductor device is described in, for example, Japanese Patent Application Laid-Open No. 1990-278171 published on November 14, 1990 in Japan. A test terminal, a test circuit, and a resistive element are provided for the semiconductor device disclosed in Japanese Patent Application Laid-Open No. 1990-278171. The semiconductor device has the test circuit serving as the resistive element between an input terminal and a power source. Further, the semiconductor device is fundamentally constructed as will be now described and as shown in Fig. 1. With reference to Fig. 1, reference numerals 11, 13, and 14 mean the input terminal, an input stage transistor, and the test terminal, respectively.

The test terminal is pulled up by a pull-up resistive element 15. Reference numeral 12 refers to the test circuit comprising a single transistor which has a great ON resistance.

The test circuit 12 is turned OFF if the test terminal 14 is opened or a high voltage is applied to the test terminal 14. On the other hand, the test circuit 12 is turned ON if a low voltage is applied to the test terminal 14. When the test circuit 12 is held ON, the test circuit 12 serves as the resistive element because it comprises the transistor having the great ON resistance. Therefore, the resistive element is disposed between the input terminal 11 and the positive power source to connect with each other so that the input terminal 11 is pulled up. Thus far, a description has been made of a case that the input terminal 11 is pulled up by the test circuit. However, with the test circuit 22 as will be described later and as shown in Fig. 2, the input terminal 21 may be pulled down. In this case, when the high voltage is applied to the test terminal 24, the input terminal 21 can be pulled down.

On the other hand, the conventional semiconductor device constructed as shown in Fig. 3 is also well-known in the art. Reference numeral 30 in Fig. 3 refers to an essential component circuit in an integrated circuit β. In this figure, terminals of an integrated circuit 30 are partially illustrated. A test mode setting terminal A serves as a terminal to input a voltage signal required for turning ON and OFF a test mode setting logic circuit 32. Signal terminals B1, B2, B3 serve as terminals to input and output a signal, and serve as terminals to set and input a voltage level which is required during the test mode.

In the integrated circuit 30, when a ground voltage (GND) is applied to the test mode setting terminal A, the test mode setting logic circuit 32 is switched over to the test mode. Accordingly, it is possible to test in the condition that the signal terminal B1 is set to a power source voltage Vcc, the signal voltage B2 is set to the ground voltage, and the signal terminal B3 is set to any reference voltage V_E. Additionally, the integrated circuit 30 leaves the test mode when the test mode setting terminal A is set to the power source voltage Vcc or is opened.

However, in the semiconductor device as disclosed in Japanese Patent Application Laid-Open No. 1990-278171, the integrated circuit can exit the test mode only when the input terminal is opened. There is a further disadvantage in the semiconductor device as disclosed in Japanese Patent Application Laid-Open No. 1990-278171. Namely, the semiconductor device can not include two or more of each circuit to set the terminal voltage to the power source voltage Vcc, to the ground voltage (GND) or to an optional voltage, respectively. Furthermore, to activate a plurality of integrated circuits β as shown in Fig. 3 in the test mode simultaneously, the respective integrated circuits β should be arranged as shown in Fig. 4. That is, it is necessary to connect the signal input terminals B1 to B3 with each other as well as the test mode setting terminals A. Thus, increasing the number of the integrated circuits β causes a complicated wiring, and requires a vast amount of labour and time. In addition, some terminals can not be possibly wired due to a restricted dimension of a package or a limited space in circumference.

If the integrated circuit β is aged in the test mode, fundamental circuits can be aged while some circuit blocks can not be aged. For example, it is impossible to age the logic circuit 31 disposed between the signal input terminals B1 to B3 and the test mode setting terminal A. The logic circuit 31 can not be activated in any mode other than the test mode. As a result, there is another drawback that the whole circuit may not provide a high reliability.

Japanese Patent Application Laid-Open No. 1986-37268 discloses an integrated circuit in accordance with the preamble of claim 1, in which two signal input terminals are respectively connected to the power supply and ground voltages of the integrated circuit when a predetermined signal is applied to a control input terminal in a test mode.

Summary of the Invention

The present invention provides the integrated circuit defined by claim 1. The sub-claims 2 to 4 are directed to preferred embodiments of the invention.

According to the present invention, the integrated circuit has a function enabling a predetermined mode of

the circuit such as a test mode to be selected when a predetermined control voltage is input through a mode switching terminal. In this mode, a respective predetermined voltage is applied to one or more signal input terminals. The integrated circuit comprises a voltage setting circuit connected to the or each signal input terminal. The voltage setting circuit is arranged to set at least one signal input terminal to receive an arbitrary reference voltage in the range from the ground voltage to the power source voltage in response to the control voltage which is input through the mode switching terminal.

In a preferred embodiment, the reference voltage is generated internally of the integrated circuit. Therefore, it is not necessary to connect the respective signal input terminals of respective integrated circuits with each other even if a number of the integrated circuits are to be tested simultaneously. Consequently, the time and wiring (space) requirements for such testing may be considerably reduced.

Brief Description of the Drawings

Fig. 1 is a circuit diagram showing a structure of a test circuit in a conventional semiconductor device;

Fig. 2 is a circuit diagram showing the semiconductor device of Fig. 1 with the test circuit pull down;

Fig. 3 is an essential block diagram showing a fundamental structure of a conventional integrated circuit;

Fig. 4 is a wiring diagram showing a plurality of conventional integrated circuits in the case of activating in a test mode at the same time;

Fig. 5 is a circuit diagram showing an internal structure of an integrated circuit of the present invention; and

Fig. 6 is a wiring diagram showing a plurality of the circuits of Fig. 5 in the case of activating in the test mode at the same time.

Description of the Preferred Embodiment

A preferred embodiment of the present invention will be described hereinafter with reference to the drawings.

Fig. 5 is a circuit diagram partially illustrating an internal structure of an integrated circuit of the present invention. The integrated circuit α of the invention has a function (a test mode) for automatically testing an operation of a circuit as in the case of the conventional integrated circuit as shown in Fig. 3. Further, when the integrated circuit α is switched over to the text mode, a signal input terminal and a mode setting terminal A are used as in the case of the conventional integrated circuit.

Unlike the conventional circuit, the circuit of the invention is provided with a voltage setting circuit 40 arranged between each terminal, i.e., the mode setting terminal A (corresponding to a mode switching input terminal) and the signal input terminals B1 to B3, and an integrated circuit 30 (corresponding to a logic circuit) to connect with each other. The voltage setting circuit 40 will be described hereinafter.

The integrated circuit of the invention is provided with an inverter 5 arranged between the mode setting terminal A and an integrated circuit 30 to connect with each other. The mode setting terminal A is connected to each gate of p-channel FETs (Field Effect Transistors) 1, 3 as well as to an input terminal of the inverter 5.

On the other hand, an output terminal of the inverter 5 is connected to each gate of n-channel FETs 2, 4 as well as to an input terminal of a test mode setting logic circuit 32 (see Fig. 3) in the integrated circuit 30. A source of the FET 2 is grounded (GND) and a drain thereof is connected to the signal terminal B2. Further, the FET 3 and the FET 4 have a shared source, and are connected to the signal terminal B3. Each drain of the FETs 3, 4 is connected to a voltage generating circuit (not shown) for generating a reference voltage (V_E: $0<V_E<V_{cc}$). In the case of the conventional circuit of Fig. 3, the reference voltage (V_E) is externally supplied to the integrated circuit. However, in the circuit of this embodiment, it is supplied by the voltage generating circuit which is separately provided in the integrated circuit.

The construction of the voltage setting circuit 40 should be changed according to a voltage which should be applied to the signal input terminals B1 to B3 during the test mode. The circuit including the FET 2 may be used if the signal terminal is set to the voltage Vcc (corresponding to the power source) or if the circuit including the FET 1 is set to the ground (GND) voltage. In addition, the inverter 5 may be omitted in case all of the signal input terminals B1 to B3 are set to the power source voltage Vcc or the ground (GND) voltage.

A description will be given of an operation in the case that the integrated circuit having the construction as set forth above is switched over to the test mode.

When the test mode setting terminal A is set to the GND voltage, in other words, a signal voltage is input through the mode setting terminal A, a voltage Vcc (corresponding to the power source) is output from the inverter 5. Accordingly, the FETs 1, 2, 3, and 4 are turned ON, respectively, since each gate voltage of the P-channel FETs 1 and 3 is set to the GND voltage while that of the n-channel FETs 2 and 4 is set to the power source voltage Vcc. As a result, the signal input terminal B1 is set to the power source voltage Vcc, the signal input terminal B2 is set to the GND voltage. Hence, the reference voltage (V_E) is applied to the signal terminal B3 by the voltage generating circuit set forth hereinbefore. Also, in the embodiment, an inverter (not shown) is separately provided in a stage preceding a circuit to restore an inverted signal since the mode setting logic circuit 32 can be naturally switched over to the test mode by the GND voltage.

If the mode setting terminal A is set to the power source voltage Vcc or is opened, the FETs 1, 2, 3, and

4 are respectively turned OFF to leave the mode. With leaving the mode, a signal can be input and output through the signal input terminals B1 to B3.

When the plurality of integrated circuits α set forth above are simultaneously operated in the test mode, the integrated circuits α are wired as shown in Fig. 6. Namely, a general wiring may be employed as long as the mode setting terminals A are communicated with each other and connected to an earthing wire.

Thus, unlike the conventional circuit, it is not necessary to connect the signal input terminals B1 to B3 with each other to operate the integrated circuit of the invention in the test mode. As a result, it is possible to reduce an operation time required for wiring, the wiring operation, and a working space required for the operation even if the number of the integrated circuit α is increased.

Further, it is not necessary to connect the signal input terminals B1 and B2 with each other even if the reference voltage V_E is obtained externally. As a result, the wiring operation can be facilitated in the circuit of the invention relative to the conventional circuit. Particularly, it is possible to avoid such a case that voltage level can not be set for the signal input terminals B1 to B3 due to, for example, a limited space.

Moreover, unlike the conventional circuit, it is possible to age the logic circuit 31 as well as the signal terminals B1 to B3 when aged in the test mode. Therefore, a higher reliability can be improved in the whole circuit.

It must be noted that the integrated circuit of the present invention may have any kind of a circuit mode to be switched over, and the number of the signal input terminals required to be set in the mode should not be limited.

Furthermore, the integrated circuit may be adapted to change the kind of circuit mode according to the voltage which is set for one or more signal input terminals. Additionally, the integrated circuit may include the signal input terminal without extending from a package thereof.

The invention may be embodied in other specific forms without departure from the scope thereof as defined by the claims.

Claims

1. An integrated circuit having a mode switching input terminal (A) and at least one signal input terminal (B1,B2,B3), the integrated circuit being switchable in response to a predetermined mode switching signal applied to said mode switching input terminal into a mode, for example a test mode, requiring the application of a predetermined voltage (Vcc,GND, V_E) to said at least one signal input terminal, wherein the integrated circuit itself incorporates a voltage setting circuit (40) responsive to said mode switching signal to supply said predetermined voltage to said at least one signal input terminal, internally of the integrated circuit, characterised in that said at least one signal input terminal comprises a first terminal (B3) requiring, in said mode, the application of a predetermined reference voltage (V_E) lying above the ground voltage and below the power source voltage of the integrated circuit, and in that said voltage setting circuit (40) includes a switch comprising complementary FETs (FET3, FET4) through which said predetermined reference voltage (V_E) can be supplied to said first terminal (B3), said switch being controlled according to said mode switching signal.

2. An integrated circuit according to claim 1, wherein a voltage generating circuit for generating said predetermined reference voltage (V_E) from said ground and power supply voltages is incorporated internally of the integrated circuit.

3. An integrated circuit according to claim 1 or claim 2, wherein said at least one signal input terminal comprises a second terminal (B1) requiring the application of a voltage corresponding to the power source voltage in said mode, and wherein said voltage setting circuit (40) includes a second switch (FET1) connected between the power source voltage (Vcc) and said second terminal, said second switch being controlled according to said mode switching signal.

4. An integrated circuit according to any of claims 1 to 3, wherein said at least one signal input terminal comprises a third terminal (B2) requiring the application of a voltage corresponding to the ground voltage in said mode, and wherein said voltage setting circuit (40) includes a third switch (FET2) connected between the ground voltage (GND) and said third terminal, said third switch being controlled according to said mode switching signal.

Patentansprüche

1. Integrierter Schaltkreis mit einem Modusumschaltungs-Eingangsanschluß (A) und mindestens einem Signal-Eingangsanschluß (B1, B2, B3), wobei der integrierte Schaltkreis in Erwiderung auf ein vorbestimmtes, an den Modusumschaltungs-Eingangsanschluß angelegtes Modusumschaltungssignal in einen Modus, beispielsweise einen Testmodus umschaltbar ist, wofür das Anlegen einer vorbestimmten Spannung (Vcc, GND, V_E) an den mindestens einen Signal-Eingangsanschluß erforderlich ist, wobei der integrierte Schaltkreis selbst einen auf das Modusumschaltungssignal ansprechenden Spannungseinstellungs-Schaltkreis (40) enthält, um die vorbestimmte Spannung innerhalb des integrierten Schaltkreises an den mindestens

einer Signal-Eingangsanschluß zu liefern.
dadurch gekennzeichnet, daß
der mindestens eine Signal-Eingangsanschluß einen ersten Anschluß (B3) aufweist, an den das Anlegen einer vorbestimmten Referenzspannung (V_E) in dem Modus erforderlich ist, die oberhalb Masse und unterhalb der Leistungsversorgungs-Spannung des integrierten Schaltkreises liegt, und wobei der Spannungseinstellungs-Schaltkreis (40) einen Schalter (FET3, FET4) mit komplementären FETs enthält, durch den die vorbestimmte Referenzspannung (V_E) an den ersten Anschluß (B3) geliefert werden kann, wobei der Schalter dem Modusumschaltungssignal entsprechend gesteuert wird.

2. Integrierter Schaltkreis nach Anspruch 1, bei welchem ein Spannungserzeugungs-Schaltkreis zum Erzeugen der vorbestimmten Referenzspannung (V_E) zwischen Masse und Leistungsversorgungs-Spannung innerhalb des integrierten Schaltkreises eingebaut ist.

3. Integrierter Schaltkreis nach Anspruch 1 oder 2, bei welchem der mindestens eine Signaleingangsanschluß einen zweiten Anschluß (B1) aufweist, an den das Anlegen einer der Leistungsversorgungs-Spannung in dem Modus entsprechenden Spannung erforderlich ist, und wobei der Spannungseinstellungs-Schaltkreis (40) einen zwischen die Leistungsversorgungs-Spannung und den zweiten Anschluß geschalteten zweiten Schalter (FET1) enthält, welcher dem Modusumschaltungssignal entsprechend gesteuert wird.

4. Integrierter Schaltkreis nach einem der Ansprüche 1 bis 3, bei welchem der mindestens eine Signaleingangsanschluß einen dritten Anschluß (B2) aufweist, an den das Anlegen einer der Leistungsversorgungs-Spannung in dem Modus entsprechenden Spannung erforderlich ist, und wobei der Spannungseinstellungs-Schaltkreis (40) einen zwischen Masse (GND) und dem dritten Anschluß geschalteten dritten Schalter (FET2) enthält, welcher dem Modusumschaltungssignal entsprechend gesteuert wird.

Revendications

1. Circuit intégré ayant une borne d'entrée de commutation de mode (A) et au moins une borne de sortie de signal (B1, B2, B3), le circuit intégré pouvant être commuté, en réponse à un signal de commutation de mode prédéterminé appliqué à ladite borne d'entrée de commutation de mode, dans un mode, par exemple un mode de test, nécessitant l'application d'une tension prédéterminée (Vcc, GND, V_E) à ladite au moins borne d'entrée de signal, ledit circuit intégré lui-même comportant un circuit de réglage de tension (40) sensible audit signal de commutation de mode pour délivrer ladite tension prédéterminée à ladite au moins borne d'entrée de signal, à l'intérieur du circuit intégré, caractérisé en ce que ladite au moins borne d'entrée de signal comprend une première borne (B3) nécessitant, dans ledit mode, l'application d'une tension de référence prédéterminée (V_E) qui se situe au-dessus de la tension de terre et au-dessous de la tension de la source d'énergie du circuit intégré, et en ce que ledit circuit de réglage de tension (40) comprend un commutateur comportant des FET complémentaires (FET3, FET4) par l'intermédiaire desquels ladite tension de référence prédéterminée (V_E) peut être délivrée à ladite première borne (B3), ledit commutateur étant commandé en fonction dudit signal de commutation de mode.

2. Circuit intégré selon la revendication 1, dans lequel un circuit générateur de tension pour générer ladite tension de référence prédéterminée (V_E) à partir des tensions de la terre et de la source d'énergie est incorporé à l'intérieur du circuit intégré.

3. Circuit intégré selon la revendication 1 ou 2, dans lequel ladite au moins borne d'entrée de signal comprend une deuxième borne (B1) nécessitant l'application d'une tension correspondant à la tension de la source d'énergie dans ledit mode, et dans lequel ledit circuit de réglage de tension (40) comprend un deuxième commutateur (FET1) connecté entre la tension (Vcc) de la source d'énergie et ladite deuxième borne, ledit deuxième commutateur étant commandé en fonction dudit signal de commutation de mode.

4. Circuit intégré selon l'une quelconque des revendications 1 à 3, dans lequel ladite au moins borne d'entrée de signal comprend une troisième borne (B2) nécessitant l'application d'une tension correspondant à la tension de terre dans ledit mode, et dans lequel ledit circuit de réglage de tension (40) comprend un troisième commutateur (FET2) connecté entre la tension de terre (GND) et ladite troisième borne, ledit troisième commutateur étant commandé en fonction dudit signal de commutation de mode.

FIG. 1 PRIOR ART

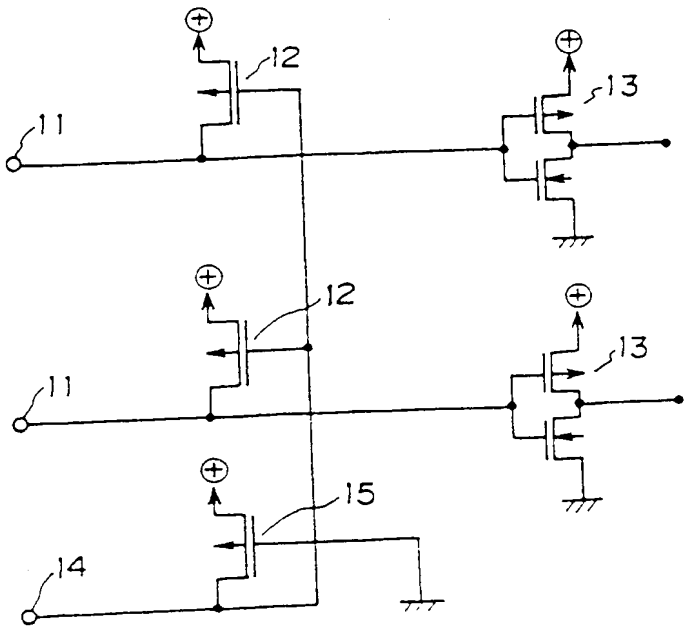

FIG. 2 PRIOR ART

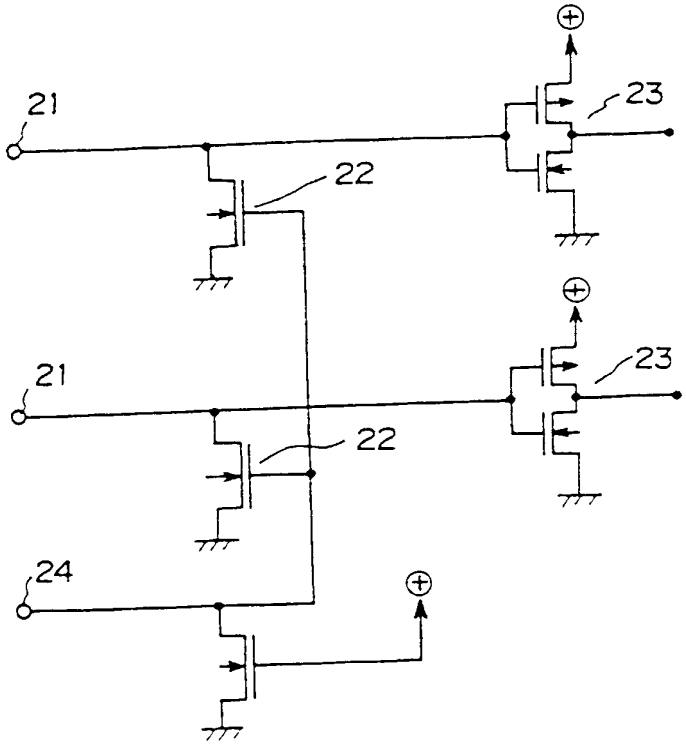

FIG. 3 PRIOR ART

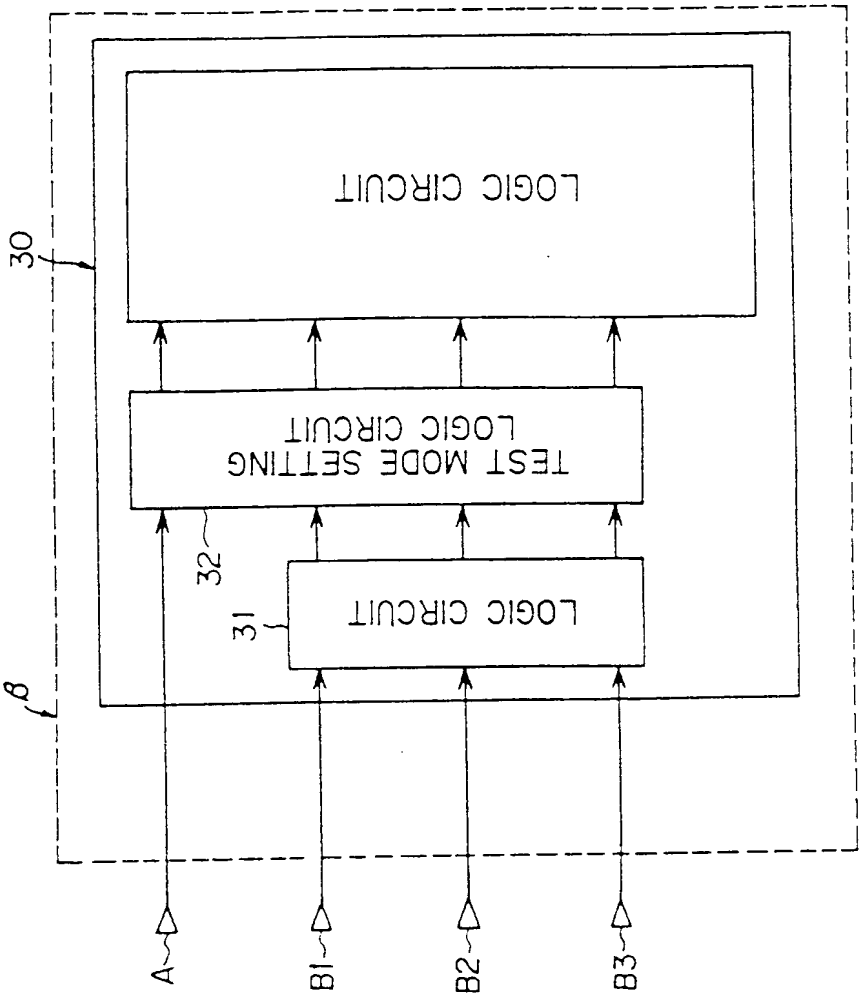

FIG. 4 PRIOR ART

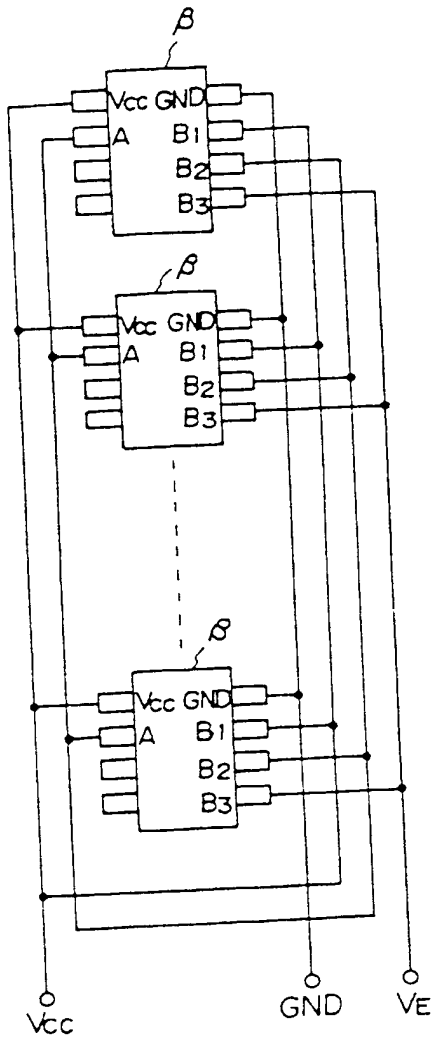

FIG. 5

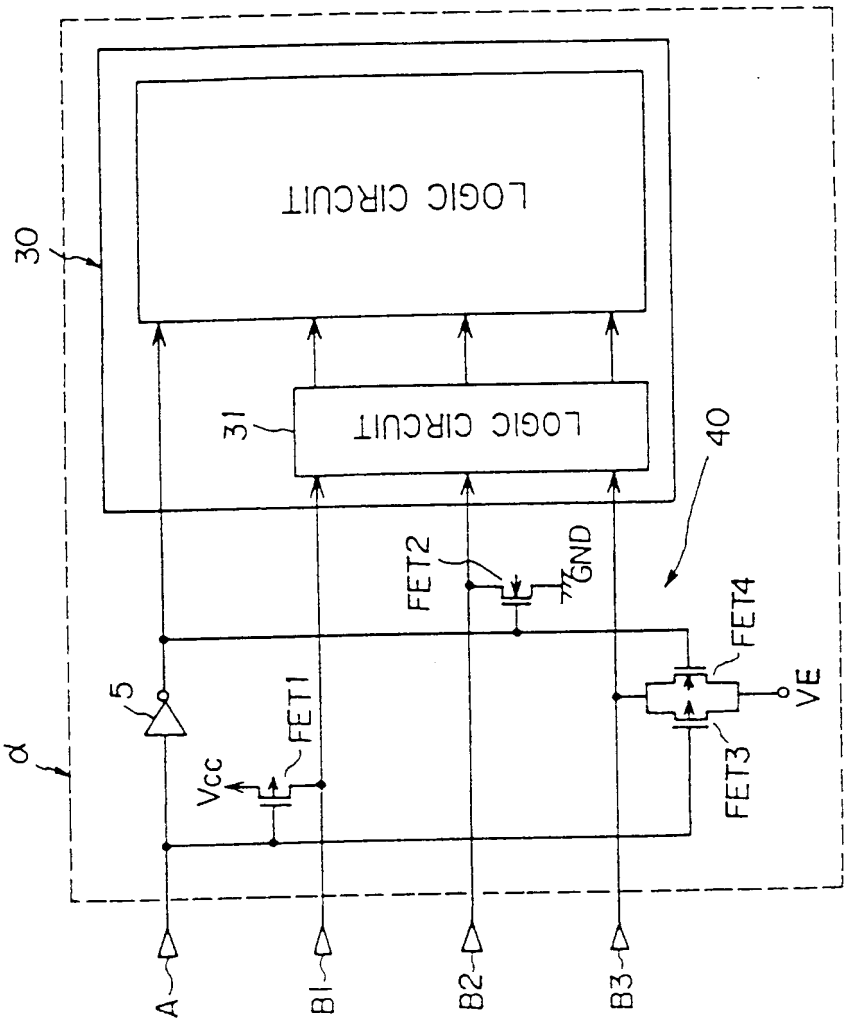
LOGIC CIRCUIT
30
LOGIC CIRCUIT
31
40
FET2
GND
FET4
VE
5
FET1
Vcc
FET3
α
A
B1
B2
B3

FIG. 6